UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/658,936	09/09/2003	Richard M. Fastow	AMD-H0561	3102

7590 08/18/2005

WAGNER, MURABITO & HAO LLP
Third Floor
Two North Market Street
San Jose, CA 95113

EXAMINER	
NGUYEN, DAO H	
ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 08/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/658,936	FASTOW ET AL.	
	Examiner	Art Unit	
	Dao H. Nguyen	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,7,8,10,12,13 and 21-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,7,8,10,12,13 and 21-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. In response to the communications dated 06/23/2005, claims 1, 3, 7, 8, 10, 12, 13, and 21-25 are active in this application.

Claims 2, 4-6, 9, 11, and 14-20 have been cancelled.

New claims 21-25 have been added.

Remarks

2. Applicant's argument(s) filed 06/23/2005, with respect to the newly amended/added claim(s) 1, 3, 7, 8, 10, 12, 13, and 21-25, have been fully considered, but they are not persuasive. See the following rejections for details.

Claim Objection

3. Claims 1 and 21 are objected to for the following reason: on claim 1, line 5, and claim 21, line 4, the limitation "said silicon dioxide layer" lack(s) an antecedent basis. This limitation is not priorly defined.

For the purpose of performing the search, Examiner assume, to the best understanding of the Examiner of what Applicant may mean, that Applicant intends to refer to the layer comprising a (first) silicon material defined on line 3 of corresponding claims.

Claim Rejections - 35 U.S.C. § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

5. Claim(s) 1, 3, 10, 12, and 21-23 are rejected under 35 U. S. C. § 102 (e) as being anticipated by U.S. Patent No. 6,713,810 to Bhattacharyya.

Regarding claim 1, Bhattacharyya discloses a flash memory cell, as shown in figs. 10-11, comprising:

a substrate comprising a source/drain regions 58;

a layer 210 comprising a silicon material (ONO material, col. 13, lines 1-8) and adjacent said substrate;

a dielectric layer 52 adjacent said silicon layer 210, said dielectric layer 52 comprising a dielectric material (Si_3N_4, col. 12, lines 55-58) having a dielectric constant ($k = 6 \sim 7$) greater than that of silicon dioxide ($k = 3.9$; for further properties of silicon dioxide and silicon nitride and their dielectric constants, see the "Semiconductor Glossary" at "http://www.semiconductorglossary.com/");

a floating gate 254 adjacent said dielectric layer 52;

an oxide-nitride-oxide (ONO) laver 208 adjacent said floating gate 254; and

a control gate 206 adjacent said ONO laver 208.

Regarding claim 3, Bhattacharyya discloses the flash memory cell wherein said silicon material 210 is selected from the group consisting of silicon dioxide, silicon oxynitride and silicon oxynitrate. See col. 13, lines 1-5.

Regarding claim 10, Bhattacharyya discloses a flash memory array comprising a memory cell, as shown in figs. 10-11, wherein the memory cell comprising:

a substrate comprising a source/drain regions 58;

a tunnel oxide layer 52 adjacent said substrate, said tunnel oxide layer 52 comprising a dielectric material (Si_3N_4, col. 12, lines 55-58) having a dielectric constant ($k = 6 \sim 7$) greater than that of silicon dioxide ($k = 3.9$; for further properties of silicon dioxide and silicon nitride and their dielectric constants, see the "Semiconductor Glossary" at "http://www.semiconductorglossary.com/");

a layer 210 comprising a silicon material (ONO material, col. 13, lines 1-8) and adjacent said tunnel oxide layer 52;

a floating gate 254 adjacent said dielectric layer 52;

an oxide-nitride-oxide (ONO) laver 208 adjacent said floating gate 254; and

a control gate 206 adjacent said ONO laver 208.

Regarding claim 12, Bhattacharyya discloses the flash memory array wherein said silicon material 210 is selected from the group consisting of silicon dioxide, silicon oxynitride and silicon oxynitrate. See col. 13, lines 1-5.

Regarding claim 21, Bhattacharrya discloses a flash memory cell, as shown in figs. 10-11, comprising:

a substrate comprising a source/drain regions 58;

a first layer (first silicon dioxide layer in the stack 210 of silicon dioxide-silicon nitride-silicon dioxide, col. 12, lines 59-65) comprising a first silicon material and adjacent said substrate;

a dielectric layer 52 adjacent said first silicon layer (first silicon dioxide layer in the stack 210 of silicon dioxide-silicon nitride-silicon dioxide), said dielectric layer 52 comprising a dielectric material (Si_3N_4, col. 12, lines 55-58) having a dielectric constant (k = 6 ~ 7) greater than that of silicon dioxide (k = 3.9; for further properties of silicon dioxide and silicon nitride and their dielectric constants, see the "Semiconductor Glossary" at "http://www.semiconductorglossary.com/");

a second layer (second silicon dioxide layer in the stack 210 of silicon dioxide-silicon nitride-silicon dioxide, col. 12, lines 59-65) comprising a first silicon material and adjacent said dielectric layer;

a floating gate 254 adjacent said dielectric layer 52;

an oxide-nitride-oxide (ONO) laver 208 adjacent said floating gate 254; and

a control gate 206 adjacent said ONO laver 208.

Regarding claim 22, Bhattacharyya discloses the flash memory cell wherein said first silicon material is selected from the group consisting of silicon dioxide, silicon oxynitride and silicon oxynitrate. See col. 12, lines 59-65.

Regarding claim 23, Bhattacharryya discloses the flash memory cell wherein said second silicon material is selected from the group consisting of silicon dioxide, silicon oxynitride and silicon oxynitrate. See col. 12, lines 59-65.

Claim Rejections - 35 U.S.C. § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim(s) 7, 8, 13, 24, and 25 are rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent No. 6,713,810 (hereafter '810), in view of U.S. Patent No. 6,784,480 (hereafter '480), both to Bhattacharyya.

Regarding claims 7, 13, and 24, in '810, Bhattacharrya discloses the flash memory cell comprising all claimed limitations, except for the dielectric material comprising a metal oxide.

In '480, Bhattacharrya discloses memory device, as shown in figs. 1, 8, comprising a substrate 102 with source/drain regions 104/108, a gate structure having a layer 128 comprising a silicon material adjacent the substrate 102, and a dielectric layer 116 adjacent the layer 128 and the substrate 102, wherein the dielectric layer 116 comprising a metal oxide (Ta_2O_5, layer 124), or a composite of a metal oxide (Ta_2O_5, layer 124) and a material selected from the group consisting of silicon dioxide, silicon oxynitride and silicon oxynitrate (SiO_2, layer 122).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Bhattacharrya described in '810 to have a dielectric layer as that described in '480 in order to obtain finite probability of directly tunneling of electrons from the floating gate to the substrate, and also to provide additional barrier to charge transport off of the floating gate toward the substrate. See col. 7, lines 55-62 of '480.

Conclusion

8. **THIS ACTION IS MADE FINAL.** A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date

the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dao Nguyen whose telephone number is (571)272-1791. The examiner can normally be reached on Monday-Friday 9:00am - 6:00pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms, can be reached on (571)272-1787. The fax numbers for all communication(s) is (571)273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571)272-1625.

David Nelms
Supervisory Patent Examiner
Technology Center 2800

Dao H. Nguyen
Art Unit 2818
August 10, 2005